Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Amended) A test pattern generation and comparison apparatus in communication with a built-in-self-test controller and functional integrated circuits , comprising:

a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits~~, whereby said test stimulus signal has a plurality of bits~~; and

a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of the bits of said multiple bit test stimulus signals as required by said functional integrated circuits.

2. (Amended) The test pattern generation and comparison apparatus of claim 1 further comprising:

a plurality of parallel-to-serial converters, ~~wherein~~ each parallel-to-serial converter is connected to one of the plurality of latency buffers, to convert said multiple bit test stimulus signals to a serialized multiple bit test stimulus signals to be scanned to a scan register of said functional integrated circuit.

3. (Amended) The test pattern generation and comparison apparatus of claim 1 wherein said background and command decoder comprises:

high level command bus decode logic ~~which decodes a high level command bus~~ for activating ~~RAM~~ control signals~~, and whereby the decode logic also controls the transfer of the~~ for controlling transfer of a background pattern of expected results to the error control module.

4. (Amended) The test pattern generation and comparison apparatus of claim 1 wherein said latency buffer comprises:

a plurality of serially connected flip-flop circuits~~, whereby~~ connected such that a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to said background and command decoder to receive one bit of said multiple bit test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, ~~whereby~~ and connected such that each subsequent flip-flop circuit of the serially

connected flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and ~~whereby~~ connected such that a last flip-flop circuit has an input connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said multiple bit test stimulus signal.

5. (Amended) The test pattern generation and comparison apparatus of claim 4 ~~whereby~~ wherein the adjusting in time of the bits of the serialized multiple bit test stimulus signals is determined by a number of flip-flop circuits in the plurality of serially connected flip-flop circuits and the number of latency buffers of the plurality of latency buffers is determined by a number of bits in the multiple bit test stimulus signals and a period of a test access clocking signal.

6. (Original) The test pattern generation and comparison apparatus of claim 5 wherein the number of flip-flop circuits is determined by the formula

$$\mathbf{N} = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking signal.

7. (Amended) The test pattern generation and comparison apparatus of claim 2 wherein the parallel-to-serial circuit comprises:

a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data input to receive one of a first portion of bits of said multiple bit test stimulus signal and a clock input ~~to receive~~ receiving a clocking signal to latch said the bit of the multiple bit test stimulus signal;

a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input to receive one of a remaining portion of bits of said multiple bit test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the multiple bit test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of flip-flops has a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

a second plurality of multiplexor circuits ~~whereby~~ each multiplexor circuit ~~has~~ having a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

8. (Amended) The test pattern generation and comparison apparatus of claim 1 further comprising:

a test response comparison circuit connected to said background and control decoder to receive an expected test response signal providing a correct response expected from said integrated circuits in response to said serialized multiple bit test stimulus signals, and connected to said integrated circuit to receive a test response signal that is the response of the integrated circuit to said serialized multiple bit test stimulus signal.

9. (Amended) The test pattern generation and comparison apparatus of claim 8 wherein the test response comparison circuit comprises:

a comparator circuit to receive the test response signal and the expected test response signal, compare said test response signal

to said expected serialized test response signal and produce a test results signal indicating functioning of said integrated circuits.

10. (Amended) The test pattern generation and comparison apparatus of claim 9 wherein said comparator circuit comprises:

[[An]] an exclusive OR and OR logic tree which compares the ~~RAM data output from the serial-to-parallel converter~~ test response signal to an expected ~~data output pattern~~ test response signal from the background data.

11. (Amended) The test pattern generation and comparison apparatus of claim 9 wherein said test response comparison circuit further comprises:

a error-handling module ~~to~~ that receives the test response signal and the expected test response signal and creates a diagnostic signal indicating a location of any fault determined to exist within said integrated circuits.

12. (Amended) The test pattern generation and comparison apparatus of claim 11 wherein said error handling module comprises:

a serial shift register composed of flip-flops~~, which~~ that are presettable from the ~~serial-to-parallel data bus from the RAM~~ test response signal, ~~and~~ said serial shift register ~~is~~ being loaded by the ~~PASS/FAIL~~ test result signal from the comparator circuit~~, and~~

~~whereby the~~ for transfer from a serial output ~~from~~ of the serial shift register ~~transfers the data~~ for diagnosis.

13. (Amended) The test pattern generation and comparison apparatus of claim 5 wherein a hardware description of said test pattern generation and comparison apparatus requires the number of bits of the multiple bit test stimulus signal and the adjusting in time of the multiple bit test stimulus signal as parameters to automatically create a physical description of said test pattern generation and comparison apparatus during an automatic physical design of said integrated circuit for placement on said semiconductor substrate.

14. (Original) The test pattern generation and comparison apparatus of claim 1 wherein said functional integrated circuits are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

15. (Amended) A built-in-self test circuit incorporated with functional integrated circuits on a semiconductor substrate to verify correctness of operation of said functional integrated circuits, comprising:

a built-in-self-test controller to provide test background and command codes indicating tests to be performed on said functional integrated circuits; and

a test pattern generation and comparison apparatus in communication with the built-in-self-test controller to receive said test background and command codes and with said functional integrated circuits to transmit at least one test stimulus signal to said integrated circuit and to receive at least one test response signal to evaluate correctness of operation of said integrated circuit, comprising:

a background and command decoder connected to receive said test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create said test response signals from said functional integrated circuits, ~~whereby said test stimulus signal has a plurality of bits~~; and

a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of the bits of said multiple bit test stimulus signals as required by said functional integrated circuits.

16. (Amended) The built-in-self test circuit of claim 15 further comprising:

a plurality of parallel-to-serial converters wherein each parallel-to-serial converter is connected to one of the plurality of latency buffers, to convert said multiple bit test stimulus to a serialized multiple bit test stimulus signals to be scanned to a scan register of said functional integrated circuit.

17. (Amended) The built-in-self test circuit of claim 15 wherein said background and command decoder comprises:

high level command bus decode logic ~~which decodes a high level command bus~~ for activating ~~RAM~~ control signals~~, and whereby the decode logic also controls the transfer of the background pattern~~for controlling transfer of a background pattern of expected results to the error control module.

18. (Amended) The built-in-self test circuit of claim 15 wherein said latency buffer comprises:

a plurality of serially connected flip-flop circuits, ~~whereby~~ connected such that a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to said background and command decoder to receive one bit of said multiple bit test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, ~~whereby~~ connected such that each subsequent flip-flop circuit of the serially connected

flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and ~~whereby~~ connected such that a last flip-flop circuit has an input connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said multiple bit test stimulus signal.

19. (Amended) The built-in-self test circuit of claim 18 ~~whereby~~ wherein the adjusting in time of the multiple bit test stimulus signals is determined by a number of flip-flop circuits in the plurality of serially connected flip-flop circuits and the number of latency buffers of the plurality of latency buffers is determined by a number of bits in the multiple bit test stimulus signals.

20. (Original) The built-in-self test circuit of claim 19 wherein the number of flip-flop circuits is determined by the formula:

$$\mathbf{N} = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking signal.

21. (Amended) The built-in-self test circuit of claim 16 wherein the parallel-to-serial circuit comprises:

a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data input to receive one of a first portion of bits of said multiple bit test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the multiple bit test stimulus signal;

a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input to receive one of a remaining portion of bits of said multiple bit test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the multiple bit test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of flip-flops ~~has~~ having a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

a second plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

22. (Amended) The built-in-self test circuit of claim 15 further comprising:

a test response comparison circuit connected to said background and control decoder to receive an expected test response signal providing a correct response expected from said integrated circuits in response to said serialized multiple bit test stimulus signals, and connected to said integrated circuit to receive a test response signal that is the response of the integrated circuit to said serialized multiple bit test stimulus signal.

23. (Original) The built-in-self test circuit of claim 22 wherein the test response comparison circuit comprises:

a comparator circuit to receive the test response signal and the expected test response signal, compare said test response signal

to said expected test response signal and produce a test results signal indicating functioning of said integrated circuits.

24. (Amended) The built-in-self test circuit of claim 23 wherein said comparator circuit comprises:

an exclusive OR and OR logic tree which compares the ~~RAM data output from the serial-to-parallel converter~~ test response signal to an expected ~~data output pattern~~ test response signal from the background data.

25. (Original) The built-in-self test circuit of claim 22 wherein said test response comparison circuit further comprises:

a error-handling module to receive the test response signal and the expected test response signal and creates a diagnostic signal indicating a location of any fault determined to exist within said integrated circuits.

26. (Amended) The built-in-self test circuit of claim 25 wherein said error handling module comprises:

a serial shift register composed of flip-flops~~, which~~ that are presettable from the ~~serial-to-parallel data bus from the RAM~~ test response signal, ~~and~~ said serial shift register ~~is~~ being loaded by the ~~PASS/FAIL~~ test result signal from the comparator~~, and whereby the~~

for transfer from a serial output ~~from~~ of the serial shift register ~~transfers the data~~ for diagnosis.

27. (Amended) The built-in-self test circuit of claim 20 wherein a hardware description of said built-in-self test circuit requires the number of bits of the multiple bit test stimulus signal and the adjusting in time of the multiple bit test stimulus signal as parameters to automatically create a physical description of said built-in-self test circuit during an automatic physical design of said integrated circuit for placement on said semiconductor substrate.

28. (Original) The built-in-self test circuit of claim 15 wherein said functional integrated circuits are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

29. (Amended) A computer implemented hardware design system ~~description coding providing a description of a computer implemented~~ having a code retention device retaining a hardware description coding of a test pattern generation and comparison circuit, which,when executed, ~~to~~ automatically creates a physical description of said ~~computer implemented~~ hardware description coding during an automatic physical design of ~~said~~ an integrated circuit for placement on ~~said~~ a semiconductor substrate, ~~whereby~~ said ~~computer implemented~~ hardware description coding ~~comprises~~comprising:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits~~, whereby said test stimulus signal has a plurality of bits~~; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of each bit of said multiple bit test stimulus signals as required by said functional integrated circuits.

30. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 29 wherein the hardware description coding further ~~comprising~~ comprises:

a descriptive coding of a plurality of parallel-to-serial converters, ~~wherein~~ each parallel-to-serial converter is connected to one of the plurality of latency buffers, to convert said multiple bit test stimulus to a serialized multiple bit test stimulus signals to be scanned to a scan register of said functional integrated circuit.

31. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 29 wherein said descriptive coding of said background and command decoder comprises:

descriptive coding of high level command bus decode logic ~~which decodes a high level command bus~~ for activating ~~RAM~~ control signals~~, and whereby the decode logic also controls the transfer of the~~ for controlling transfer of a background pattern of expected results to the error control module.

32. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 29 wherein said a descriptive coding of the latency buffer comprises:

a descriptive coding of a plurality of serially connected flip-flop circuits, ~~whereby~~ connected such that a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to said background and command decoder to receive one bit of said multiple bit test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, ~~whereby~~ connected such that each subsequent flip-flop circuit of the serially connected flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and ~~whereby~~ connected such that a last

flip-flop circuit has an input connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said multiple bit test stimulus signal.

33. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 32 ~~whereby~~ wherein the adjusting in time of the multiple bit test stimulus signals is determined by a number of flip-flop circuits in the plurality of serially connected flip-flop circuits and the number of latency buffers of the plurality of latency buffers is determined by a number of bits in the multiple bit test stimulus signals.

34. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 33 wherein the number of flip-flop circuits is determined by the formula:

$$\mathbf{N} = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking signal.

35. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 30 wherein the parallel-to-serial circuit comprises:

a descriptive coding of a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data input to receive one of a first portion of bits of said multiple bit test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the multiple bit test stimulus signal;

a descriptive coding of a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input to receive one of a remaining portion of bits of said multiple bit test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the multiple bit test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

a descriptive coding of a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of flip-flops ~~has~~ having a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal

to latch the output of one of the first plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

a descriptive coding of a second plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

36. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 29 further comprising:

a descriptive coding of a test response comparison circuit connected to said background and control decoder to receive an expected test response signal providing a correct response expected from said integrated circuits in response to said multiple bit test stimulus signals, and connected to said integrated circuit to receive a test response signal that is the response of the integrated circuit to said multiple bit test stimulus signal.

37. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 36 wherein the descriptive coding of the test response comparison circuit comprises:

a descriptive coding of a comparator circuit to receive the test response signal and the expected test response signal, compare said test response signal to said expected test response signal and produce a test results signal indicating functioning of said integrated circuits.

38. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 37 wherein said descriptive coding of comparator circuit comprises:

descriptive coding of an exclusive OR and OR logic tree which compares the ~~RAM data output from the serial-to-parallel converter~~ test response signal to an expected ~~data output pattern~~ test response signal from the background data.

39. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 37 wherein said descriptive coding of test response comparison circuit further comprises:

a descriptive coding of an error-handling module to receive the test response signal and the expected test response signal and creates

a diagnostic signal indicating a location of any fault determined to exist within said integrated circuits.

40. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 39 wherein said descriptive coding of error handling module comprises:

descriptive coding of a serial shift register composed of flip-flops~~, which~~ that are presettable from the ~~serial-to-parallel data bus from the~~ ~~RAM~~ test response signal, ~~and~~ said serial shift register ~~is~~ being loaded by the ~~PASS/FAIL~~ test result signal from the comparator~~,~~ ~~and whereby the~~ for transfer from a serial output from the shift register ~~transfers the data~~ for diagnosis.

41. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 33 wherein said hardware description coding of said test pattern generation and comparison apparatus requires the number of bits of the multiple bit test stimulus signal and the adjusting in time of the multiple bit test stimulus signal as parameters to automatically create the physical description of said test pattern generation and comparison apparatus during an automatic physical design of said integrated circuit for placement on said semiconductor substrate.

42. (Amended) The computer implemented hardware design system ~~description coding~~ of claim 29 wherein said functional integrated circuits

are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

43. (Amended) A data retention medium readable by a computer system containing a hardware description coding of a test pattern generation and comparison circuit, which, when exectuted, ~~providing a description of a data retention medium to~~ automatically creates a physical description of said ~~data retention medium~~ hardware description coding during an automatic physical design of ~~said~~ an integrated circuit for placement on ~~said~~ a semiconductor substrate, ~~whereby~~ said hardware description coding ~~comprises~~ comprising:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits~~, whereby said test stimulus signal has a plurality of bits~~; and

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said

multiple bit test stimulus signals as required by said functional integrated circuits.

44. (Amended) The data retention medium of claim 43 further comprising:

a descriptive coding of a plurality of parallel-to-serial converters wherein each parallel-to-serial converter is connected to one of the plurality of latency buffers, to convert said multiple bit test stimulus to **[[a]]** serialized multiple bit test stimulus signals to be scanned to a scan register of said functional integrated circuit.

45. (Amended) The data retention medium of claim 43 wherein said a descriptive coding of background and command decoder comprises:

descriptive coding of a high level command bus decode logic ~~which decodes a high level command bus~~ for activating ~~RAM~~ control signals~~, and whereby the decode logic also controls the transfer of the background pattern~~ for controlling transfer of a background pattern of expected results to the error control module.

46. (Amended) The data retention medium of claim 43 wherein said a descriptive coding of latency buffer comprises:

a descriptive coding of a plurality of serially connected flip-flop circuits, ~~whereby~~ connected such that a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to

said background and command decoder to receive one bit of said multiple bit test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, ~~whereby~~ connected such that each subsequent flip-flop circuit of the serially connected flip-flop circuits has an output connected to the input of a following flip-flop circuit of said plurality of serially connected flip-flop circuits, and ~~whereby~~ connected such that a last flip-flop circuit has an input connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said multiple bit test stimulus signal.

47. (Amended) The data retention medium of claim 46 ~~whereby~~ wherein the adjusting in time of the multiple bit test stimulus signals is determined by a number of flip-flop circuits in the plurality of serially connected flip-flop circuits and the number of latency buffers of the plurality of latency buffers is determined by a number of bits in the multiple bit test stimulus signals.

48. (Original) The data retention medium of claim 47 wherein the number of flip-flop circuits is determined by the formula:

$$\mathbf{N} = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

λ is the adjusting in time, and

ϕ is the period of the test access clocking signal.

49. (Amended) The data retention medium of claim 44 wherein the parallel-to-serial circuit comprises:

a descriptive coding of a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data input to receive one of a first portion of bits of said multiple bit test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the multiple bit test stimulus signal;

a descriptive coding of a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input to receive one of a remaining portion of bits of said multiple bit test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the multiple bit test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

a descriptive coding of a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of flip-flops ~~has~~ having a data input

connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

a descriptive coding of a second plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

50. (Amended) The data retention medium of claim 43 further comprising:

a descriptive coding of a test response comparison circuit connected to said background and control decoder to receive an expected test response signal providing a correct response expected from said integrated circuits in response to said multiple bit test stimulus signals, and connected to said integrated circuit to receive a test response signal that is the response of the integrated circuit to said multiple bit test stimulus signal.

51. (Original) The data retention medium of claim 50 wherein the descriptive coding of the test response comparison circuit comprises:

a descriptive coding of a comparator circuit to receive the test response signal and the expected test response signal, compare said test response signal to said expected test response signal and produce a test results signal indicating functioning of said integrated circuits.

52. (Amended) The data retention medium of claim 51 wherein said descriptive coding of comparator circuit comprises:

descriptive coding of an exclusive OR and OR logic tree which compares the ~~RAM data output from the serial-to-parallel converter~~ test response signal to an expected ~~data output pattern~~ test response signal from the background data.

53. (Amended) The data retention medium of claim 50 wherein said descriptive coding of test response comparison circuit further comprises:

a descriptive coding of an error-handling module to receive the test response signal and the expected test response signal and creates a diagnostic signal indicating a location of any fault determined to exist within said integrated circuits.

54. (Amended) The data retention medium of claim 53 wherein said descriptive coding of error handling module comprises:

descriptive coding of a serial shift register composed of flip-flops~~, which~~ that are presettable from the ~~serial-to-parallel data bus from the~~ ~~RAM~~ test response signal, ~~and~~ said serial shift register ~~is~~ being loaded by the ~~PASS/FAIL~~ test result signal from the comparator~~,~~ ~~and whereby the~~ for transfer from a serial output ~~from~~ of the serial shift register ~~transfersthe data~~ for diagnosis.

55. (Amended) The data retention medium of claim 46 wherein said hardware description coding of said test pattern generation and comparison apparatus requires the number of bits of the multiple bit test stimulus signal and the adjusting in time of the multiple bit test stimulus signal as parameters to automatically create the physical description of said test pattern generation and comparison apparatus during an automatic physical design of said integrated circuit for placement on said semiconductor substrate.

56. (Original) The data retention medium of claim 43 wherein said functional integrated circuits are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

57. (Amended) A method for generation of test patterns to be communicated to integrated circuits and comparison of test response patterns

communicated from said integrated circuit to verify function of said integrated circuits, comprising the steps of:

receiving a test pattern command indicating which tests ~~are~~ to be performed are communicated to said integrated circuit;

receiving a background pattern code indicating a pattern of multiple bit test stimulus signals to be communicated to said integrated circuit;

decoding said test pattern command and said background pattern code to create said multiple bit test stimulus signals;

adjusting a timing relation of said multiple bit test stimulus signals to provide correct timing relationships for said multiple bit test stimulus signals; and

communicating said multiple bit test stimulus signals to said integrated circuit.

58. (Amended) The method of claim 57 further comprising the step of:

converting said multiple bit test stimulus signals to a serial test stimulus signal;

59. (Amended) The method of claim 58 wherein communicating the serialized multiple bit test stimulus signals comprises the step of:

scanning said serialized multiple bit test stimulus signals to a scan register of said integrated circuit.

60. (Amended) The method of claim 58 wherein converting said multiple bit test stimulus signals is accomplished in a parallel-to-~~parallel~~serial converter comprising:

a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data input to receive one of a first portion of bits of said multiple bit test stimulus signal and a clock input to receive a clocking signal to latch said first portion of the bits of the multiple bit test stimulus signal;

a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input to receive one of a remaining portion of bits of said multiple bit test stimulus signal, second input to receive an output of one of the first plurality of flip-flops, and a select input to receive a loading signal to selectively transfer the remaining bit of the multiple bit test stimulus signal and the output of one of the first plurality of flip-flops to an output of said multiplexor circuit;

a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of flip-flops has a data input connected to an output of one of the first plurality of multiplexor circuits, and a clock input connected to receive the clocking signal to latch the output of one of the first

plurality of multiplexor circuits to the output of said flip-flop of said plurality of flip-flops; and

a second plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit ~~has~~ having a first input connected to a first flip-flop of the plurality of flip-flops, second input connected to a second flip-flop of the second plurality of flip-flops, and a select input connected to the clocking signal to alternately transfer the first input to an output of said multiplexor circuits and the second input to the output, as said clocking signal changes from a first level to a second level and from the second level to the first level.

61. (Amended) The method of claim 57 wherein adjusting the timing relationship of said multiple bit test stimulus signals is accomplished in a latency buffer comprising:

a plurality of serially connected flip-flop circuits, ~~whereby~~ connected such that a first flip-flop circuit of said plurality of serially connected flip-flop circuits has a data input connected to said background and command decoder to receive one bit of said multiple bit test stimulus signal and an output connected to a subsequent flip-flop circuit of the serially connected flip-flop circuits, ~~whereby~~ connected such that each subsequent flip-flop circuit of the serially connected flip-flop circuits has an output connected to the input of a following

flip-flop circuit of said plurality of serially connected flip-flop circuits, and ~~whereby~~ connected such that a last flip-flop circuit has an input connected to an output of a previous flip-flop circuit and an output containing a delayed bit of said multiple bit test stimulus signal.

62. (Amended) The method of claim 57 further comprising the steps of:

creating an expected test response signal from said test pattern command and said background pattern code;

receiving the test response signals from the integrated circuit in response to said multiple bit test stimulus signal;

comparing said test response signal to said expected test response signal;

if said test response signal and expected test response signal indicate said integrated circuit is functioning, communicating a favorable test signal; and

if said test response signal and expected test response signal indicate said integrated circuit is not functioning, communicating an unfavorable test signal.

63. (Amended) The method of claim 61 wherein ~~said comparator~~ comparing said test response signal is accomplished by a comparator comprising:

an exclusive OR and OR logic tree which compares the ~~RAM dataoutput from the serial-to-parallel converter~~ test response signal to an expected ~~data output pattern~~ test response signal from the background data.

64. (Amended) The method of claim 57 further comprising the step of:

converting said test response signal to a parallel test response signal for comparison with the expected test response signal.

65. (Amended) The method of claim 64 wherein said converting is accomplished by a serial-to-parallel conversion circuit comprising:

four flip-flops per serial input ~~where~~ connected such that the output of the first flip-flop transfers to the second flip-flop and the third flip-flop whose output is the second parallel bit and ~~whereby~~ the second flip-flop transfers to the fourth flip-flop whose output is the first parallel output bit.

66. (Original) The method of claim 64 further comprising the step of:

evaluating the comparison of the test response signal and the expected test response signal to identify a fault location within said integrated circuit if said test response signal and expected test response signal indicate said integrated circuit is not functioning.

67. (Amended) The method of claim 66 where in said evaluating is accomplished in an error handling module comprising:

a serial shift register composed of flip-flops~~, which~~ that are presettable from the ~~serial-to-parallel data bus from the RAM~~ test response signal, ~~and~~ said serial shift register is loaded by the ~~PASS/FAIL~~ test result signal from the comparator~~, and whereby the~~ for transfer from a serial output ~~from~~ of the serial shift register ~~transfersthe data~~ for diagnosis.

68. (Original) The method of claim 57 wherein said functional integrated circuits are selected from a group of integrated circuits consisting of logic circuits and memory array circuits.